CLAIMS:

1. A semiconductor processing method of forming integrated circuitry comprising:

forming memory circuitry and peripheral circuitry over a substrate, the peripheral circuitry comprising first and second type MOS transistors; and

conducting second type halo implants into the first type MOS transistors in less than all peripheral MOS transistors of the first type.

2. The semiconductor processing method of claim 1, wherein the second type is p-type.

3. The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

4. The semiconductor processing method of claim 1, wherein:

the second type is p-type; and

the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

5. In a common masking step and in a common implant step, conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

6. The method of claim 5, wherein said three devices comprise peripheral circuitry.

7. The method of claim 5, wherein said three devices comprise NMOS field effect transistors.

8. The method of claim 5, wherein said three devices comprise NMOS field effect transistors comprising peripheral circuitry.

9. The method of claim 5, wherein said three devices comprise PMOS field effect transistors.

10. The method of claim 5, wherein said three devices comprise PMOS field effect transistors comprising peripheral circuitry.

11. The method of claim 5, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.

12. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

13. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

14. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

15. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

16. In a common masking step and in a common implant step, conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

17. The method of claim 16, wherein the at least some of the devices forming memory access devices receive halo implants on a bitline contact side of the devices.

18. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of n-type transistor devices over a substrate, said n-type devices comprising memory array circuitry and peripheral circuitry, individual n-type transistor devices having source regions and drain regions;

partially masking at least some individual memory array devices and peripheral circuitry n-type transistor devices; and

with said at least some of the memory array and peripheral circuitry n-type transistor devices being partially masked, conducting a halo implant for unmasked portions of said at least some peripheral circuitry n-type transistor devices.

19. The semiconductor processing method of claim 18, wherein the masking comprises masking storage node portions of one of the source region and drain region and not bitline contact portions of the other of the source region and drain region for said at least some individual memory array circuitry n-type transistor devices.

20. The semiconductor processing method of claim 18, wherein the masking comprises masking majority portions of one of the source region and drain region and not majority portions of the other of the source region and drain region for said at least some individual peripheral circuitry n-type transistor devices.

21. The semiconductor processing method of claim 18, wherein the masking comprises masking one of the source region and drain region and not the other of the source region and drain region for said at least some individual peripheral circuitry n-type transistor devices.

22. The semiconductor processing method of claim 18, wherein the masking comprises masking the source regions of said at least some individual peripheral circuitry n-type transistor devices.

23. The semiconductor processing method of claim 18, wherein the masking comprises masking the drain regions of said at least some individual peripheral circuitry n-type transistor devices.

24. The semiconductor processing method of claim 18, wherein the masking comprises (a) masking portions of only one of the source region and drain region for some of the at least some individual peripheral circuitry n-type transistor devices, and also (b) masking both source regions and drain regions for other individual peripheral circuitry n-type transistor devices.

25. The semiconductor processing method of claim 24, wherein said masking of the portions of only one of the source region and drain region comprises masking an entirety of said portions of only one of the source region and drain region for said at least some individual peripheral circuitry n-type transistor devices.

26. The semiconductor processing method of claim 18, wherein the masking comprises (a) masking portions of only one of the source region and drain region for some of the at least some individual peripheral circuitry n-type transistor devices, and also (b) leaving source regions and drain regions exposed for other individual peripheral circuitry n-type transistor devices.

27. The semiconductor processing method of claim 18, wherein the masking comprises (a) masking portions of only one of the source region and drain region for some of the at least some individual peripheral circuitry n-type transistor devices, and also (b) masking both source regions and drain regions for other individual peripheral circuitry n-type transistor devices, and (c) leaving source regions and drain regions exposed for different other individual peripheral circuitry n-type transistor devices.

28. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of n-type transistor devices over a substrate comprising memory array circuitry and peripheral circuitry, individual n-type transistor devices having source regions and drain regions;

masking at least a portion of one of the source and drain regions for at least some of the peripheral circuitry n-type transistor devices, and exposing at least a portion of the other of the source and drain regions for said at least some peripheral circuitry n-type transistor devices; and

conducting a halo implant of the exposed portions of the other of the source and drain regions.

29. The semiconductor processing method of claim 28, wherein the masking comprises masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices.

30. The semiconductor processing method of claim 28, wherein the masking comprises exposing the entire portion of the other of said source and drain regions for said at least some peripheral circuitry n-type transistor devices.

31. The semiconductor processing method of claim 28, wherein the masking comprises:

masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices; and

exposing the entire portion of the other of said source and drain regions for said at least some peripheral circuitry n-type transistor devices.

32. The semiconductor processing method of claim 28, wherein the masking comprises also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices.

33. The semiconductor processing method of claim 28, wherein the masking comprises leaving both source regions and drain regions for other peripheral circuitry n-type transistor devices exposed.

34. The semiconductor processing method of claim 28, wherein the masking comprises:

also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices; and

leaving both source regions and drain regions for different other peripheral circuitry n-type transistor devices exposed.

35. The semiconductor processing method of claim 28, wherein the masking comprises:

masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices;

also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices; and

leaving both source regions and drain regions for different other peripheral circuitry n-type transistor devices exposed.

36. The semiconductor processing method of claim 28, wherein the masking comprises:

masking the entire portion of the one source and drain region for said at least some of the peripheral circuitry n-type transistor devices;

exposing the entire portion of the other of said source and drain regions for said at least some peripheral circuitry n-type transistor devices;

also masking both source regions and drain regions for other peripheral circuitry n-type transistor devices; and

leaving both source regions and drain regions for different other peripheral circuitry n-type transistor devices exposed.

37. A semiconductor processing method of forming integrated circuitry comprising:

forming a plurality of NMOS field effect transistor devices over a substrate comprising memory array circuitry and peripheral circuitry, individual NMOS transistor devices having source regions and drain regions;

forming a mask over the substrate, the mask (a) exposing source and drain regions of first NMOS transistor devices, (b) covering source and drain regions of second NMOS transistor devices, and (c) partially exposing only a portion of third NMOS transistor devices; and

with the mask in place, conducting a halo implant.

38. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing an entirety of one of the source and drain regions and not an entirety of the other of the source and drain regions for the third NMOS transistor devices.

39. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing one of the source and drain regions and not the other of the source and drain regions for the third NMOS transistor devices.

40. The semiconductor processing method of claim 37, wherein the forming of the mask to partially expose only a portion of the third NMOS transistor devices comprises exposing a portion of one of the source and drain regions and not the other of the source and drain regions for the third NMOS transistor devices.

41. A method of improving DRAM storage cell retention time comprising conducting, in a common masking step and in a common implant step, a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to each device one of two or more different respective threshold voltages, at least some of the devices forming memory access devices, wherein the at least some of the devices forming memory access devices receive halo implants on a bit line contact side of the devices.

42. The method of claim 41 wherein the halo implant is performed prior to formation of sidewall spacers in the memory access devices.

43. The method of claim 41 wherein the halo implant is performed after formation of sidewall spacers in the memory access devices.

44. The method of claim 41 wherein the halo implant is accompanied with an n-minus implant on the bit line contact side.

45. The method ov claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

46. A method of improving DRAM storage cell retention time comprising forming memory access devices having different implants and hence different junction structures on a bitline contact side and a storage node side respectively.

47. The method of claim 46 wherein forming memory access devices includes:

performing, during a masking and implant step, a one-sided halo implant on the bitline contact side; and

performing, during the masking and implant step, an n-minus implant on the bitline contact side.

48. The method of claim 47, wherein performing a one-sided halo implant is performed prior to formation of sidewall spacers.

49. The method of claim 46, wherein the storage node side is masked during a one-sided halo implant on the bitline contact side.

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